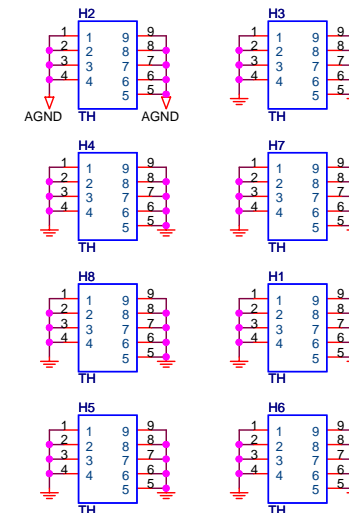


```
Mode B internal pull-up
SEL24_48 internal pull-up
(1:24MHz / 0:48MHz)
```

	ModeA	ModeB	Pin7	Pin8	Pin11
(Default)	0	0	HTTCLK1	HTTCLK2	PCICLK1
	<b>0</b>	<b>1</b>	<b>HTTCLK1</b>	<b>HTTCLK2</b>	<b>HTTCLK3</b>
	1	0	PCICLK8	PCICLK9	PCICLK1
	1	1	HTTCLK1	PCICLK9	PCICLK1

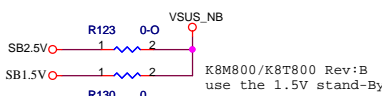
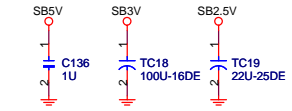
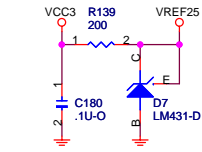
```
FS0, 1, 2  internal pull-up
FS3 internal pull-down
```

	Bit4	Bit3	Bit2	Bit1	CPU	HTT	PCT
	FS3	FS2	FS1	FS0	MHz	MHz	MHz
	0	0	0	0			
	0	0	0	1			
	0	0	1	0			
	0	0	1	1	202.00	67.33	33.6
	0	1	0	0			
	0	1	0	1			
	0	1	1	0			
(Default)	<b>0</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>200.40</b>	<b>66.80</b>	<b>33.4</b>
	1	0	0	0			
	1	0	0	1			
	1	0	1	0	210.00	70.00	35.0
	1	0	1	1			
	1	1	0	0			
	1	1	0	1			
	1	1	1	0			
	1	1	1	1			



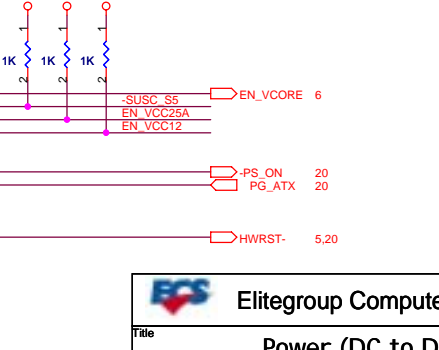
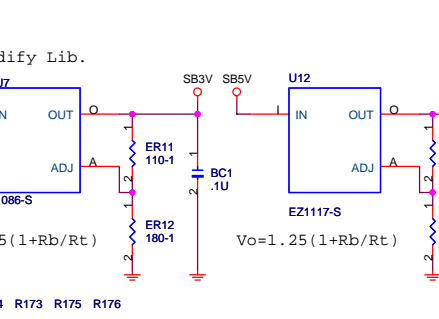
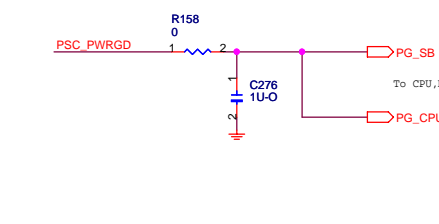
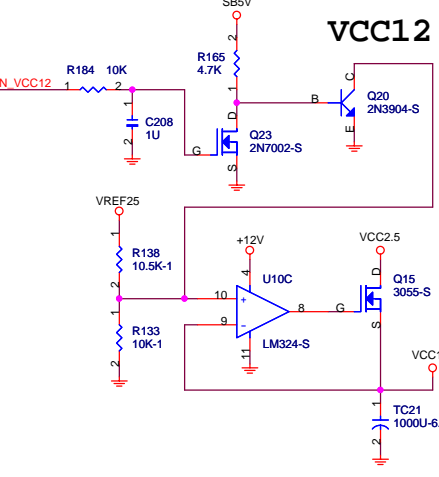
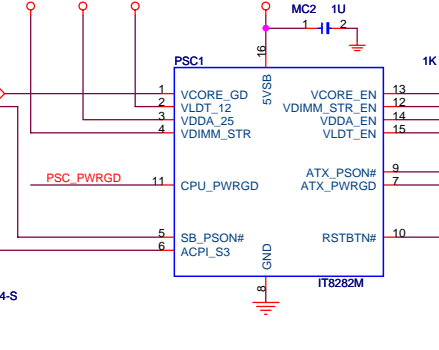
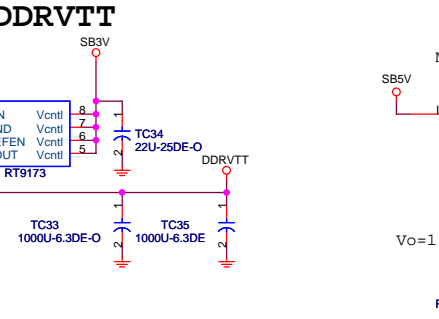
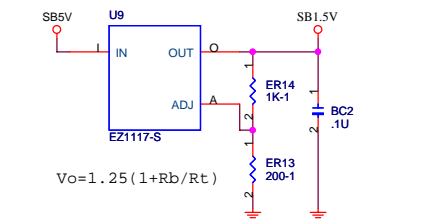
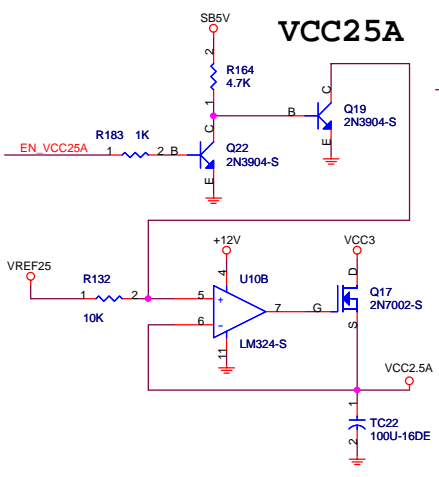
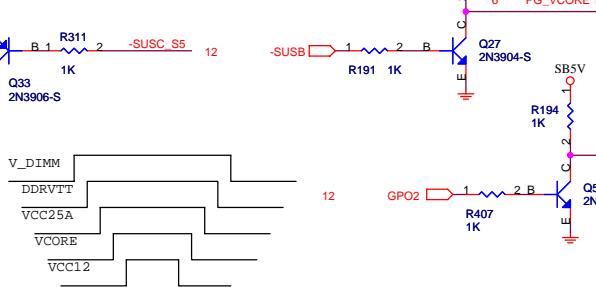
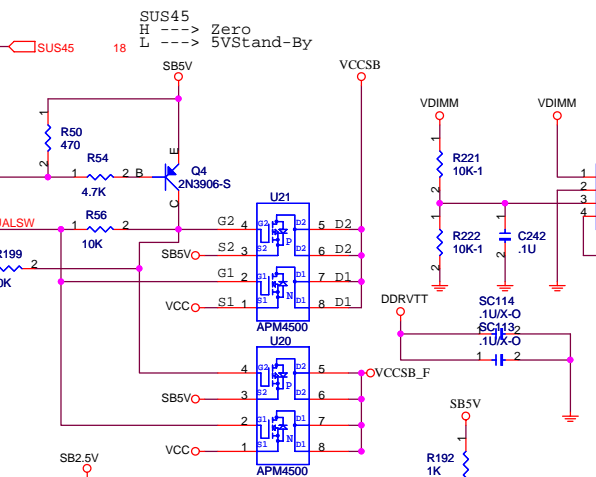
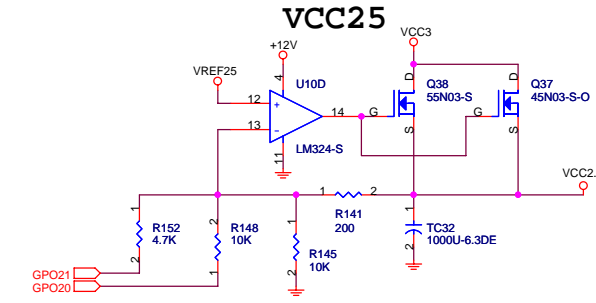
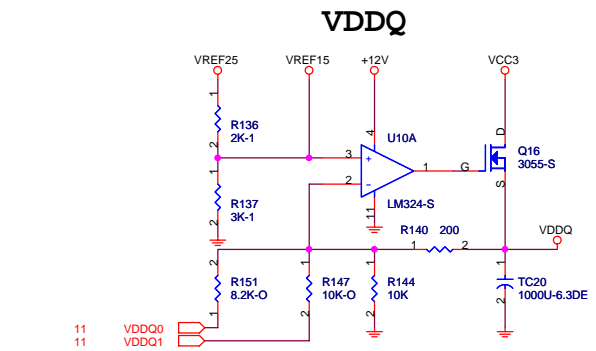
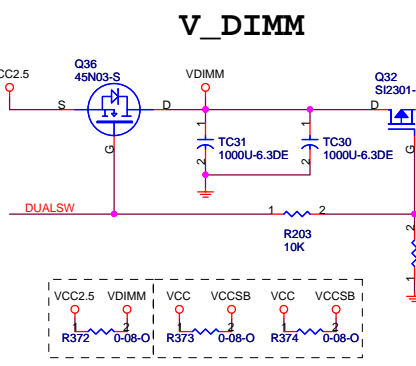
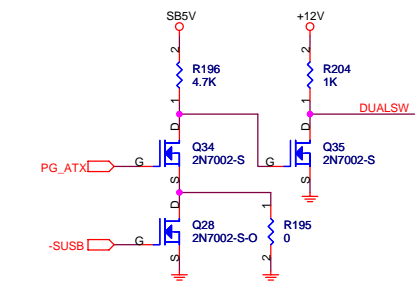


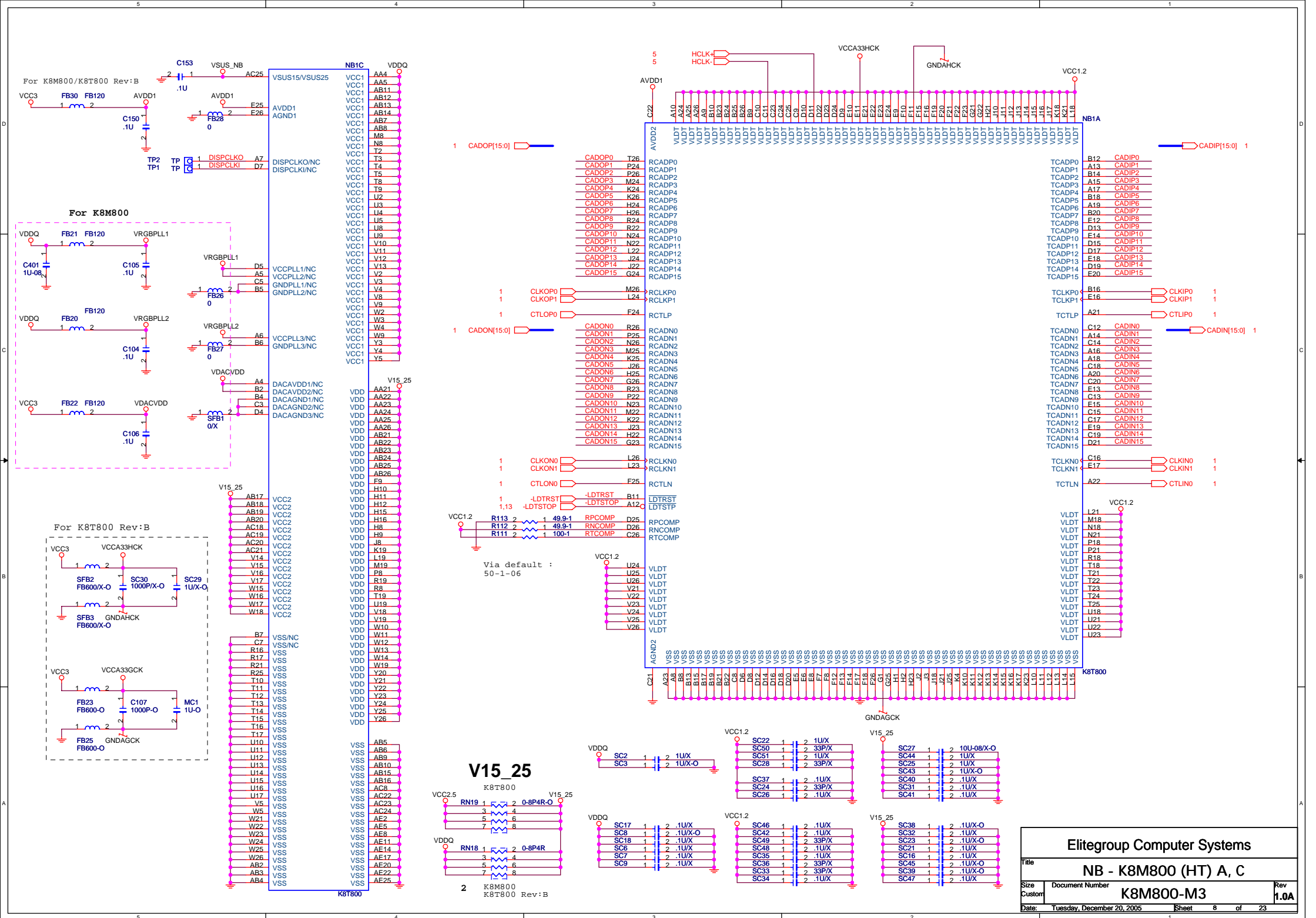




**K8T800/K8M800**

	VSUS_NB
K8T800	2.5V
K8M800	1.5V
K8T800B	1.5V







For K8M800: R61=90.9  
For K8T800: R61=140

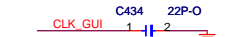
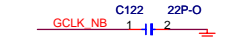
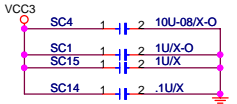
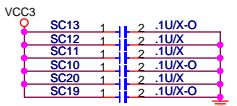
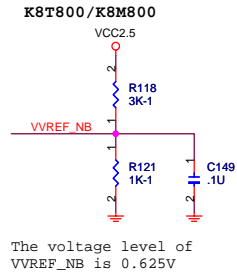
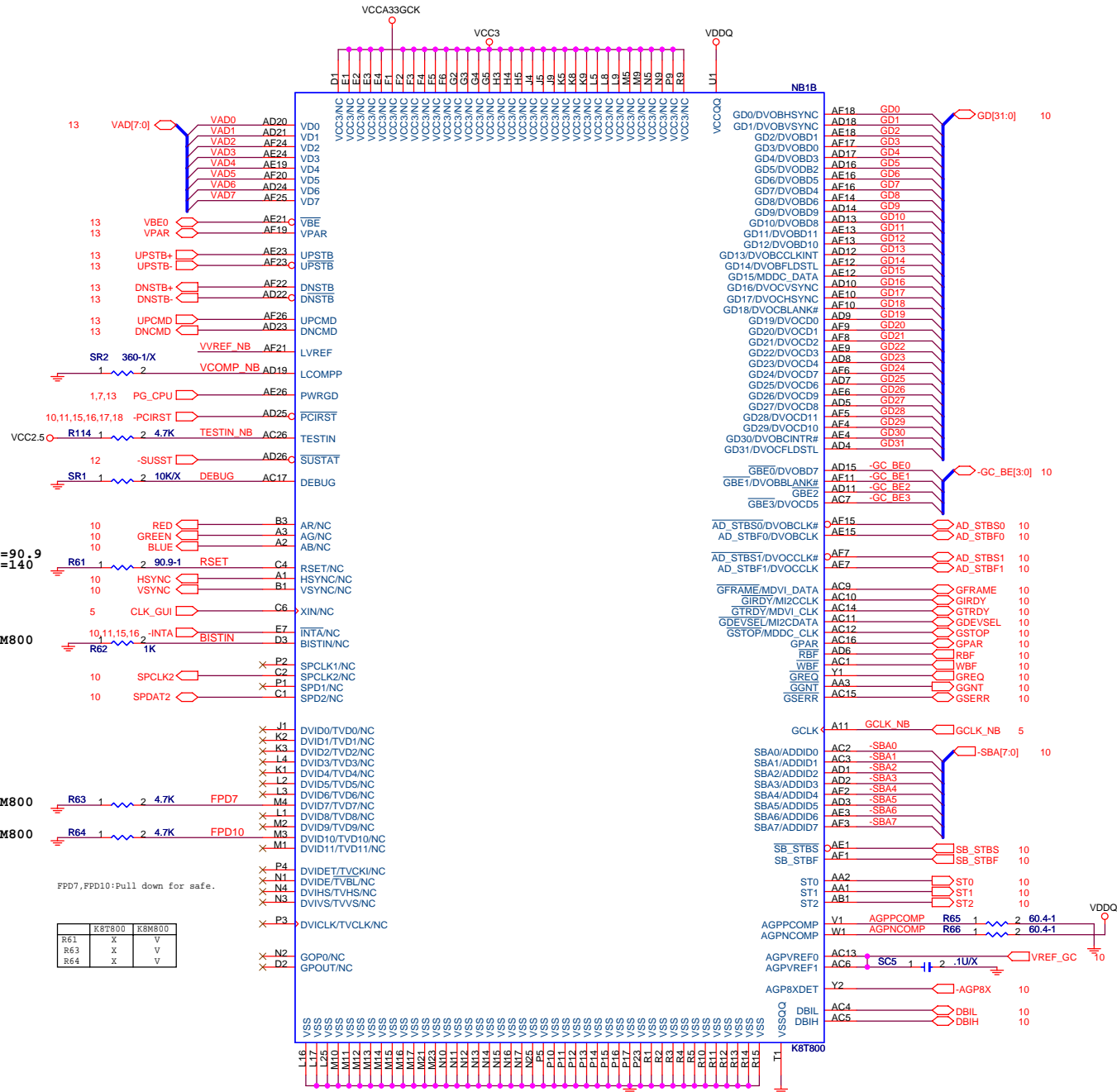
For K8M800

For K8M800

For K8M800

FPD7,FPD10: Pull down for safe.

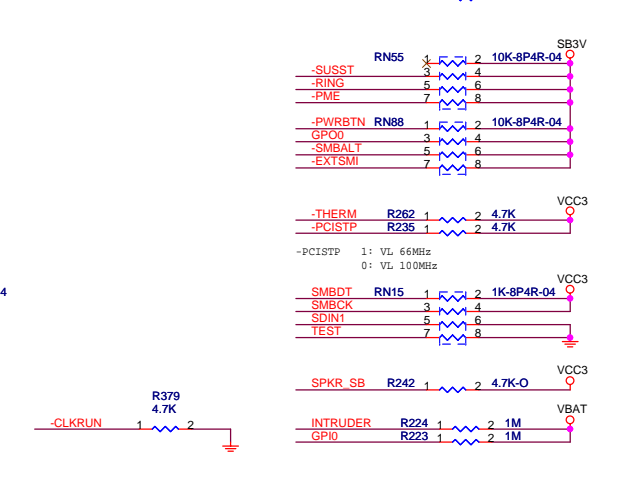
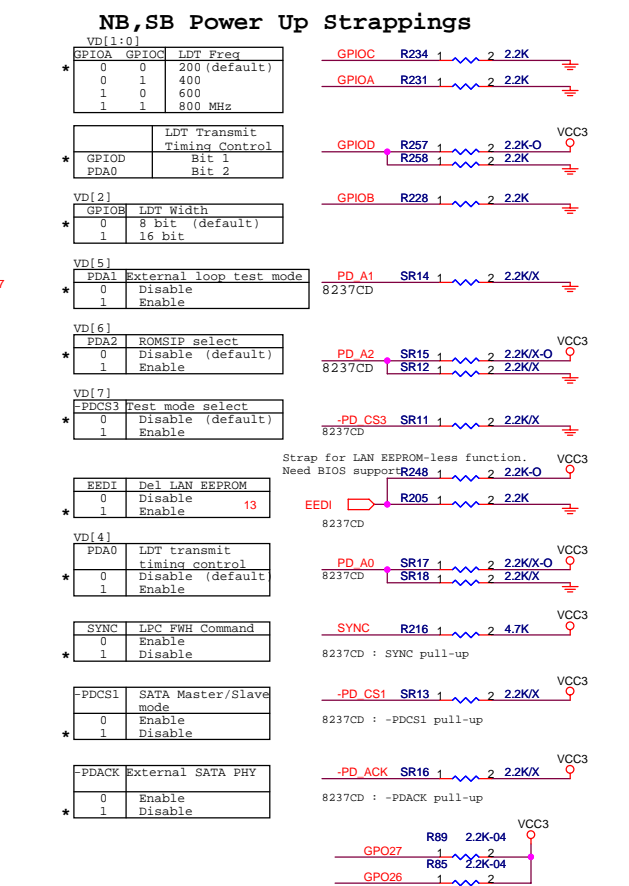
	K8T800	K8M800
R61	X	V
R63	X	V
R64	X	V

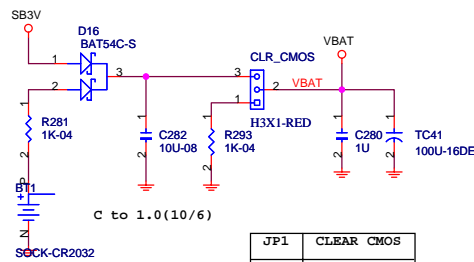
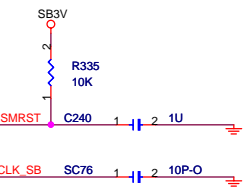
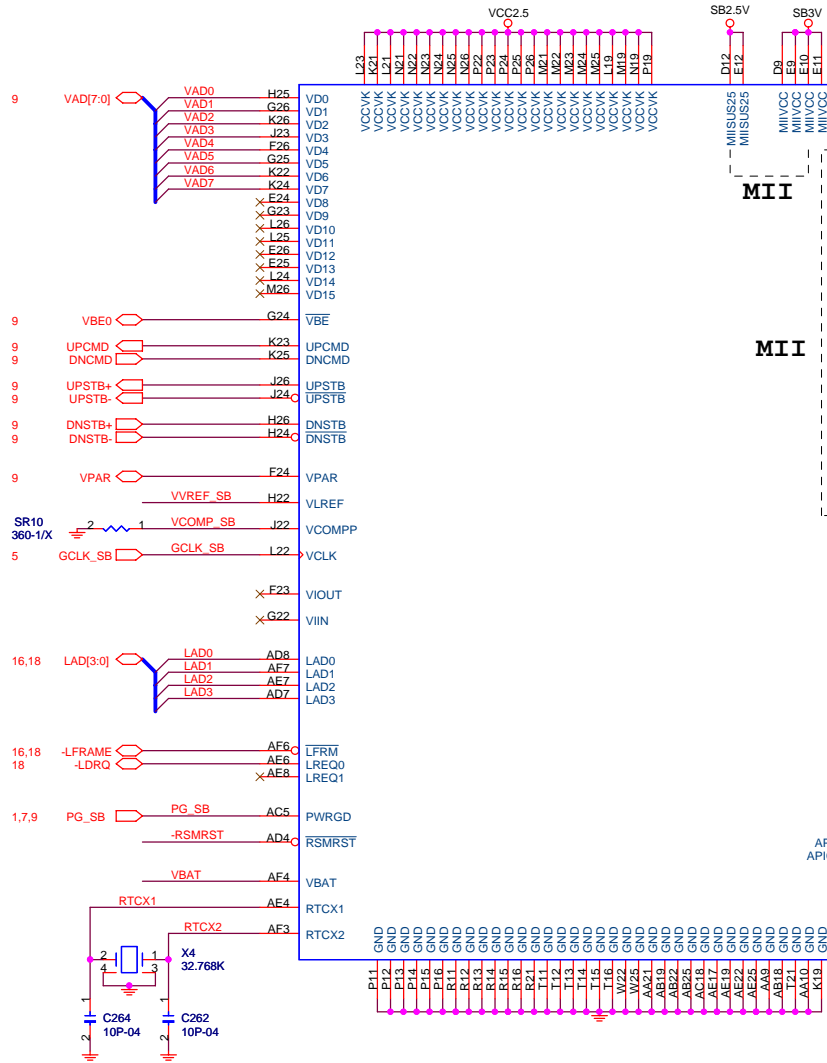


	VREF_GC
4X	0.75V
8X	0.35V



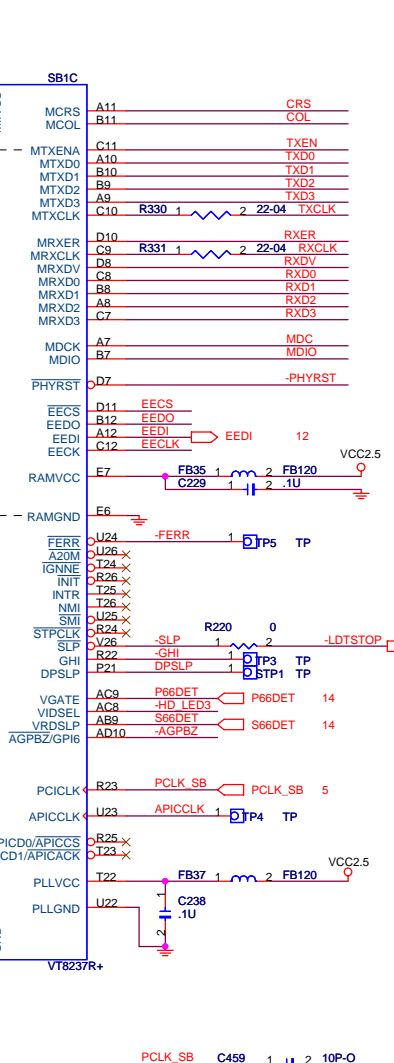




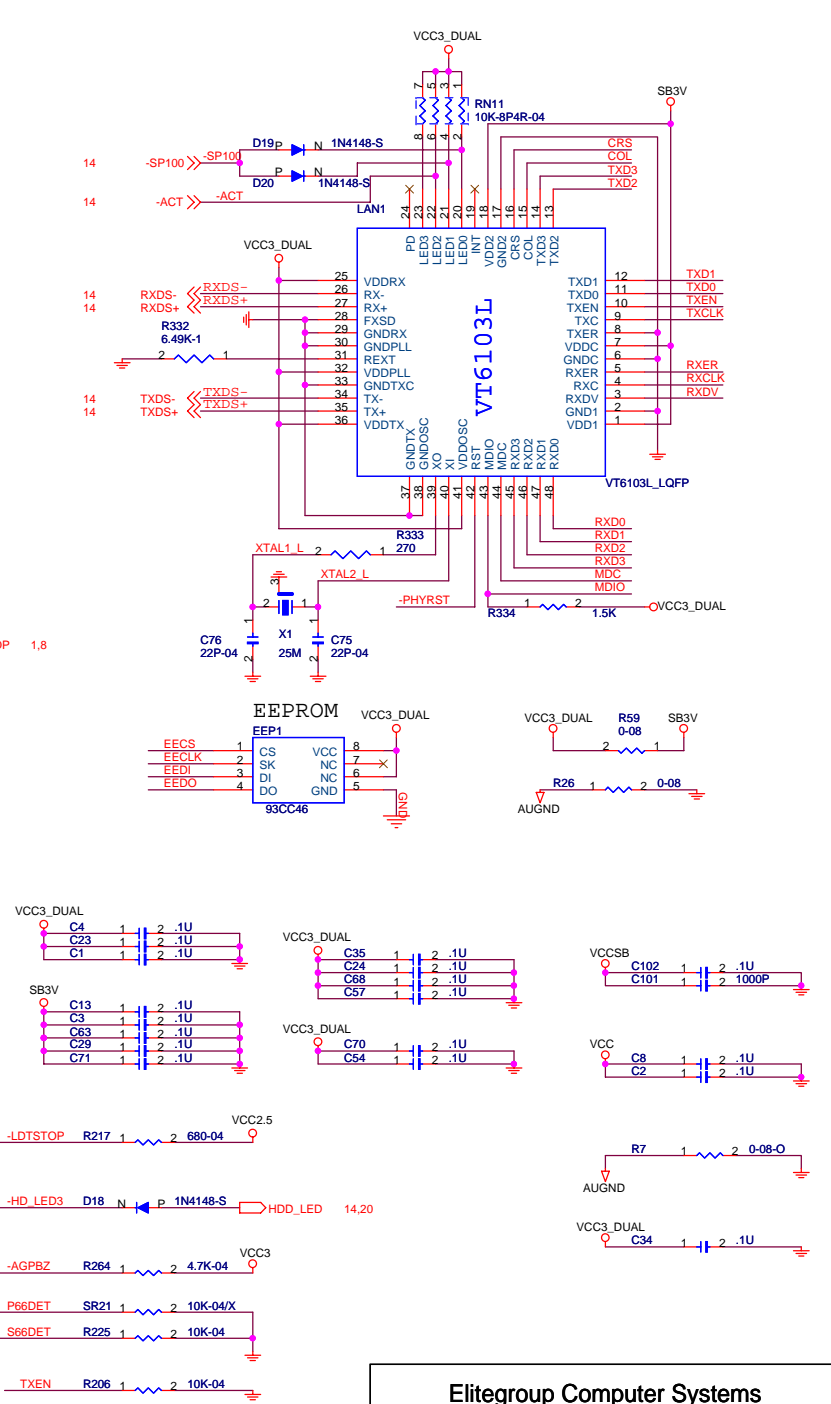


JP1	CLEAR CMOS
1-2	CLRAR
2-3	NORMAL

(Default)



K8T800/K8M800			
	VVREF_SB	Rv	
K8T800	0.625V	1K-1-06	
K8M800	0.3V	422-1-06	



Elitegroup Computer Systems

File

SB - VT8237C (V-Link, LPC & MII)

Size

Custom

Document Number

K8M800-M3

Rev

1.0A

Date:

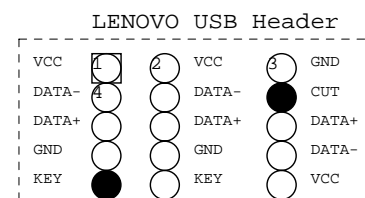
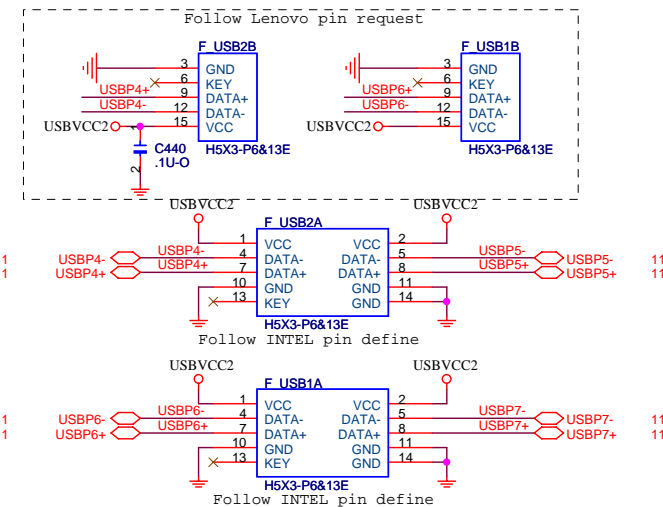
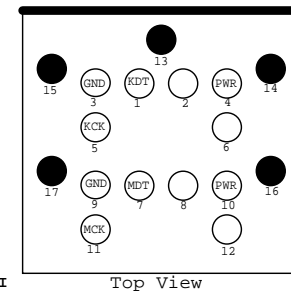
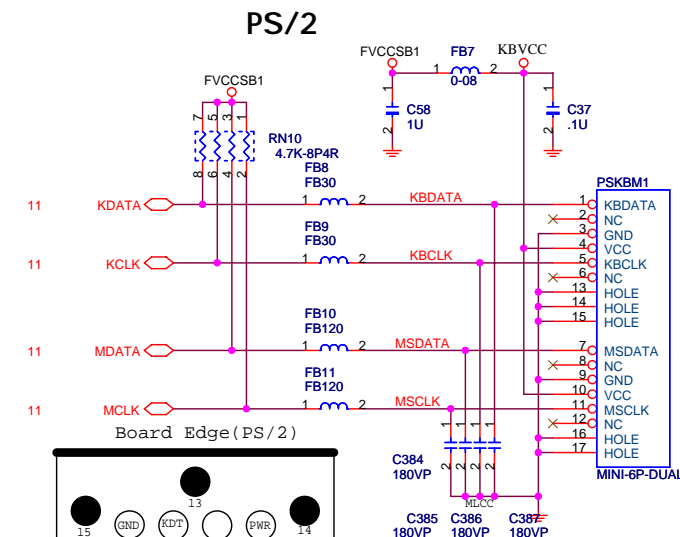
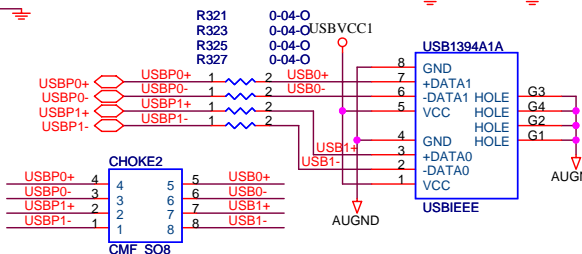
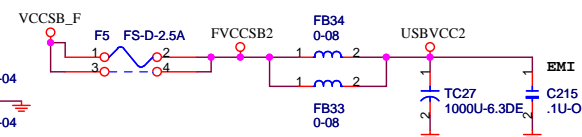
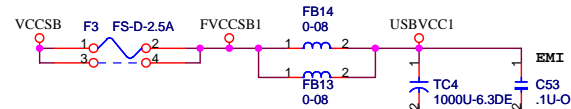
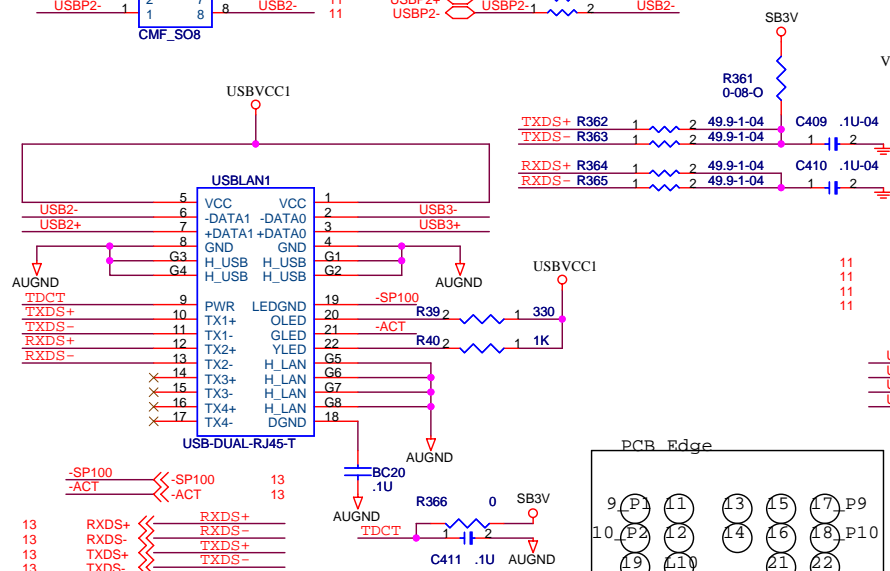
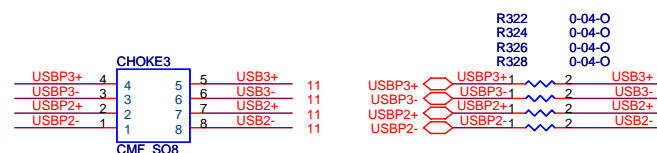
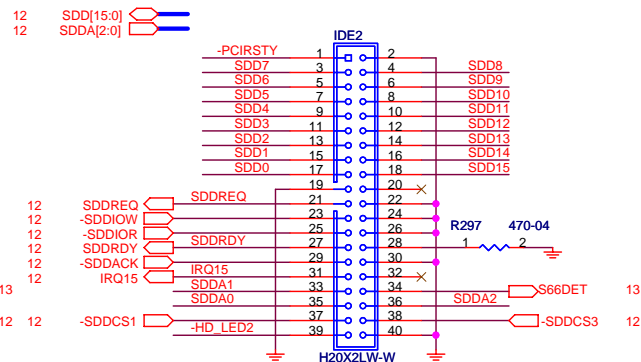
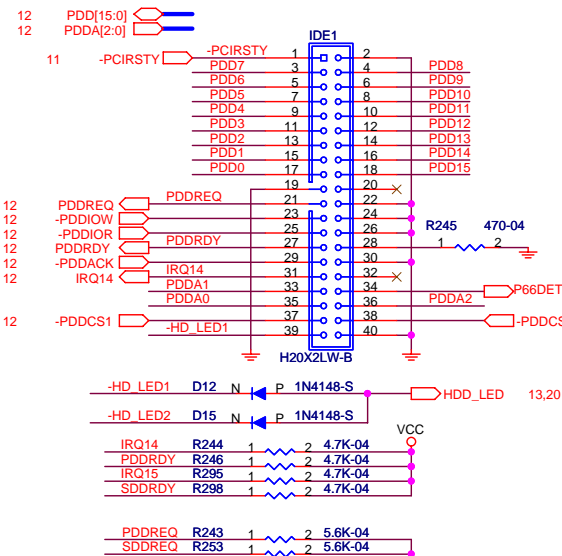
Tuesday, December 20, 2005

Sheet

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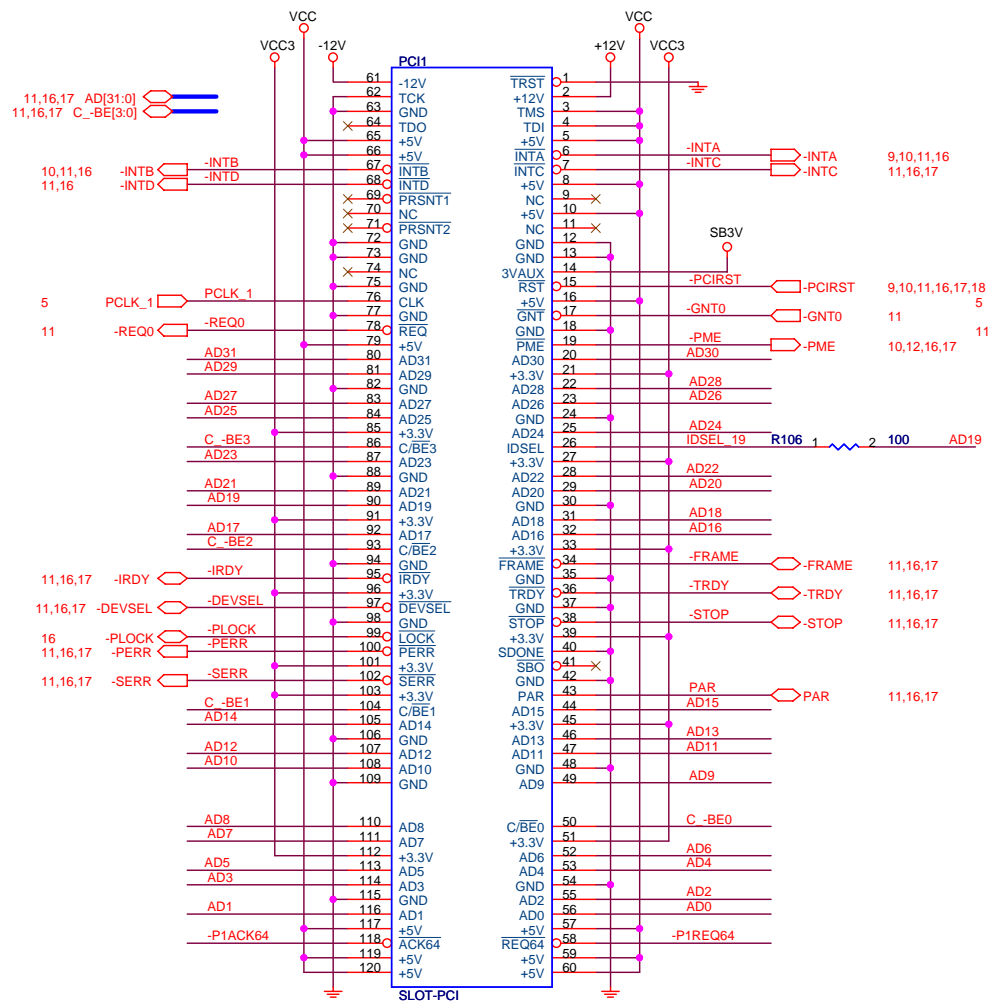
of

23

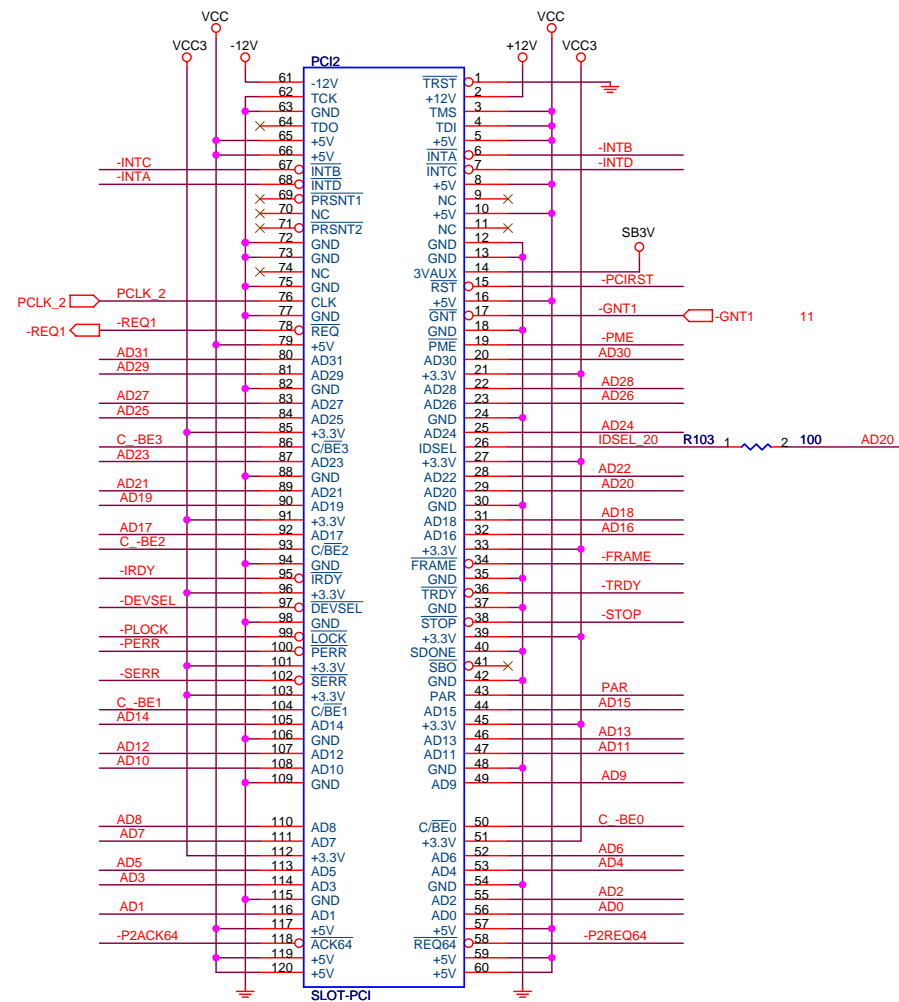
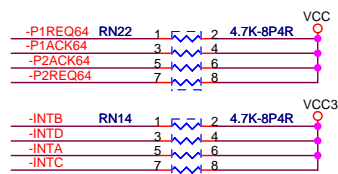
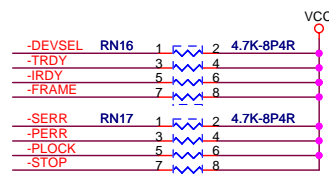


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Title PS/2, USB, I DE			
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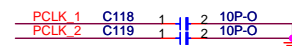


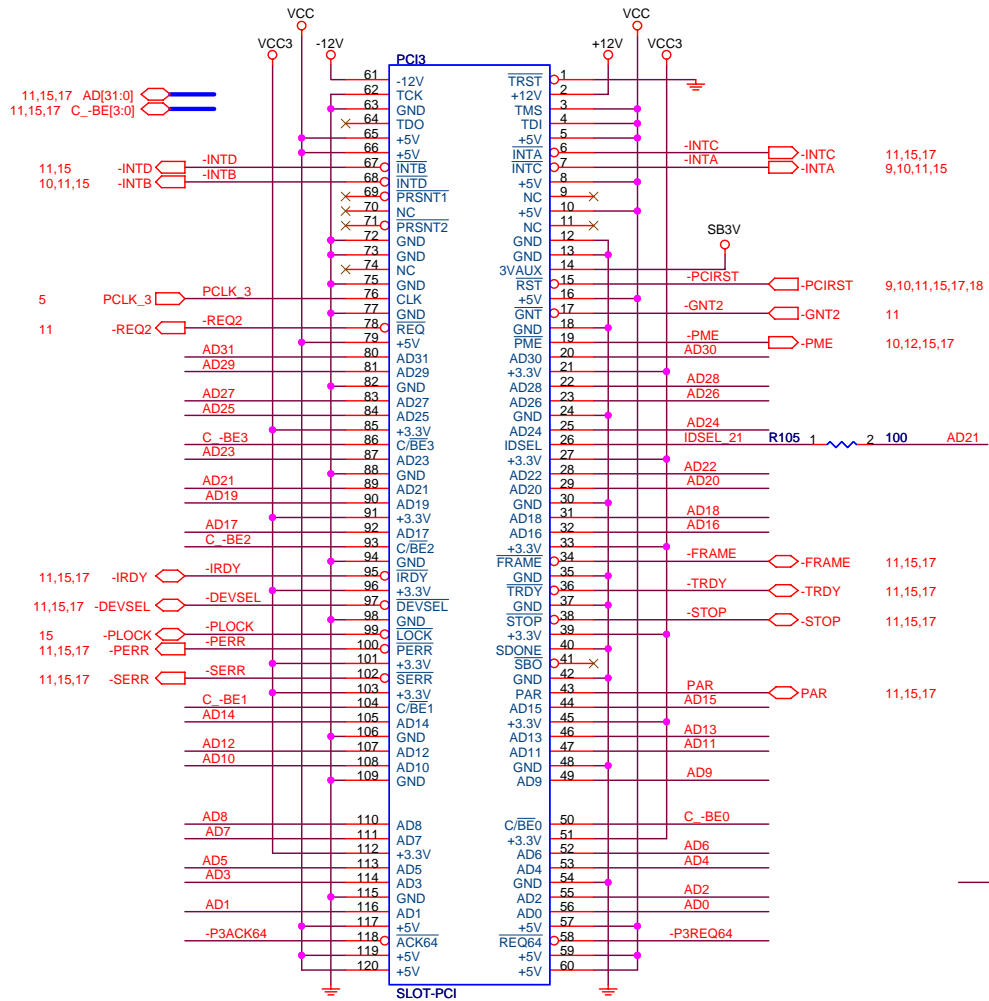


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IDSEL:AD19

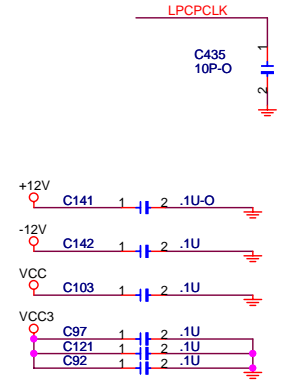
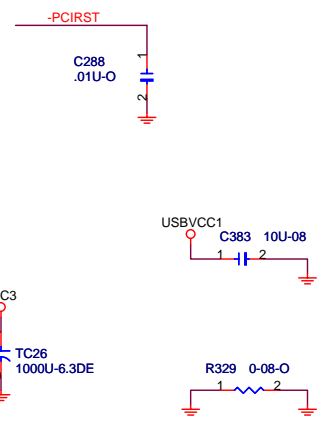
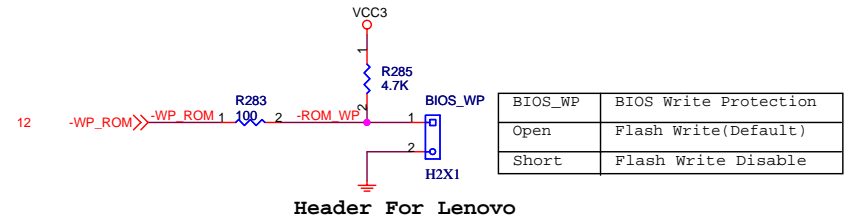
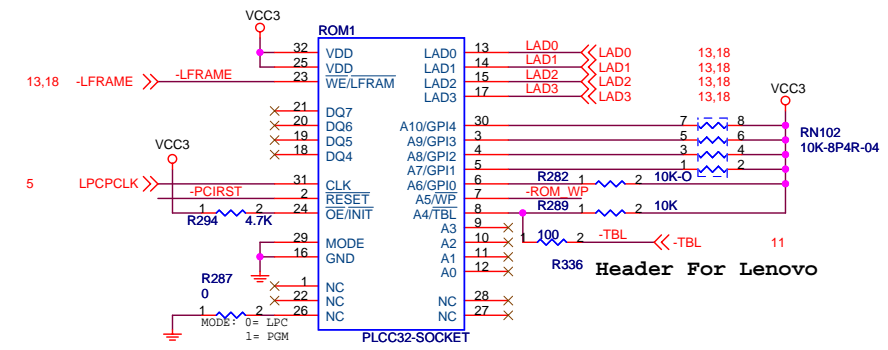
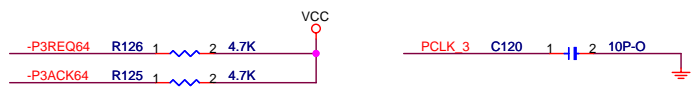


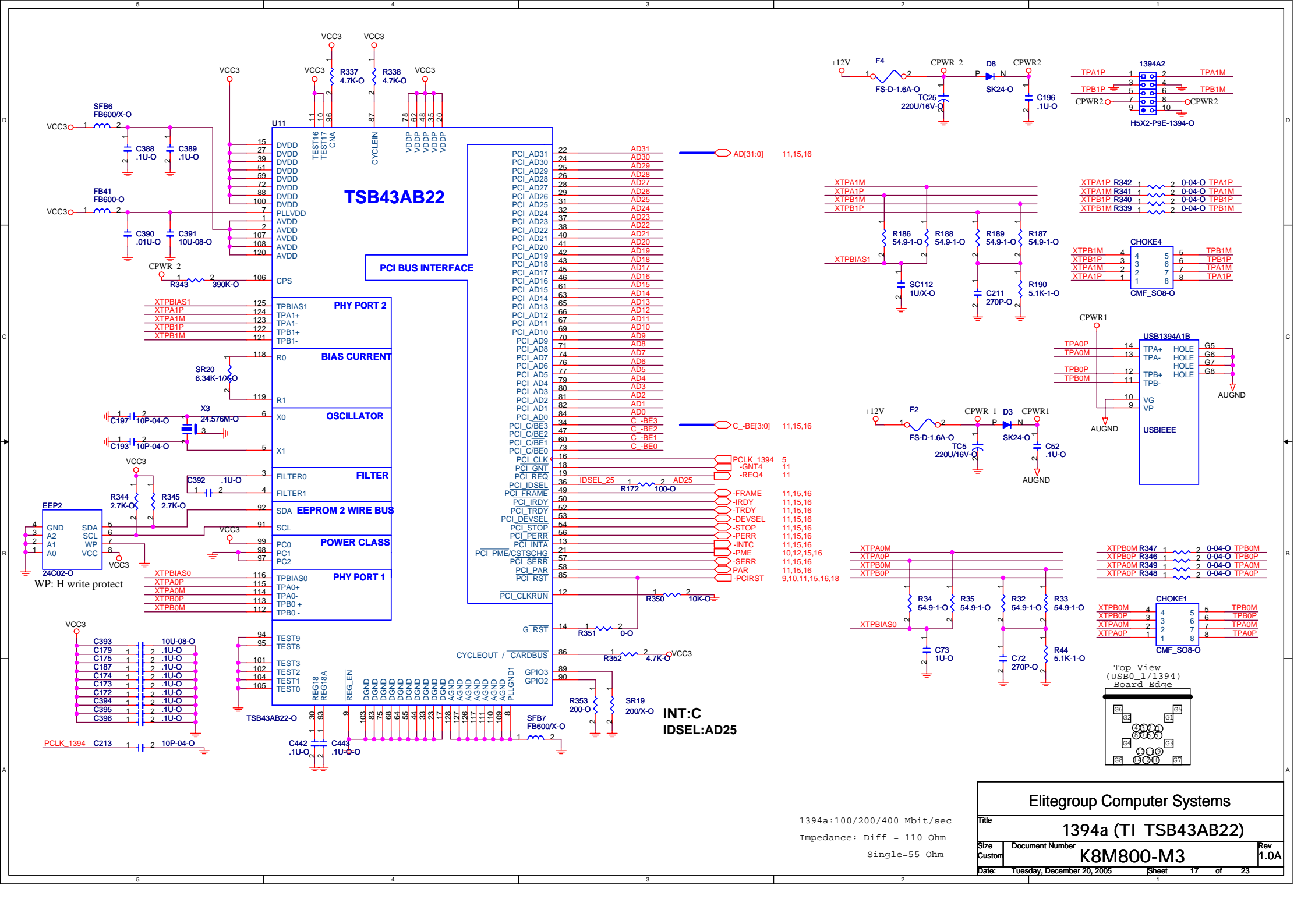
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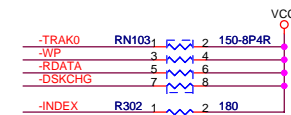
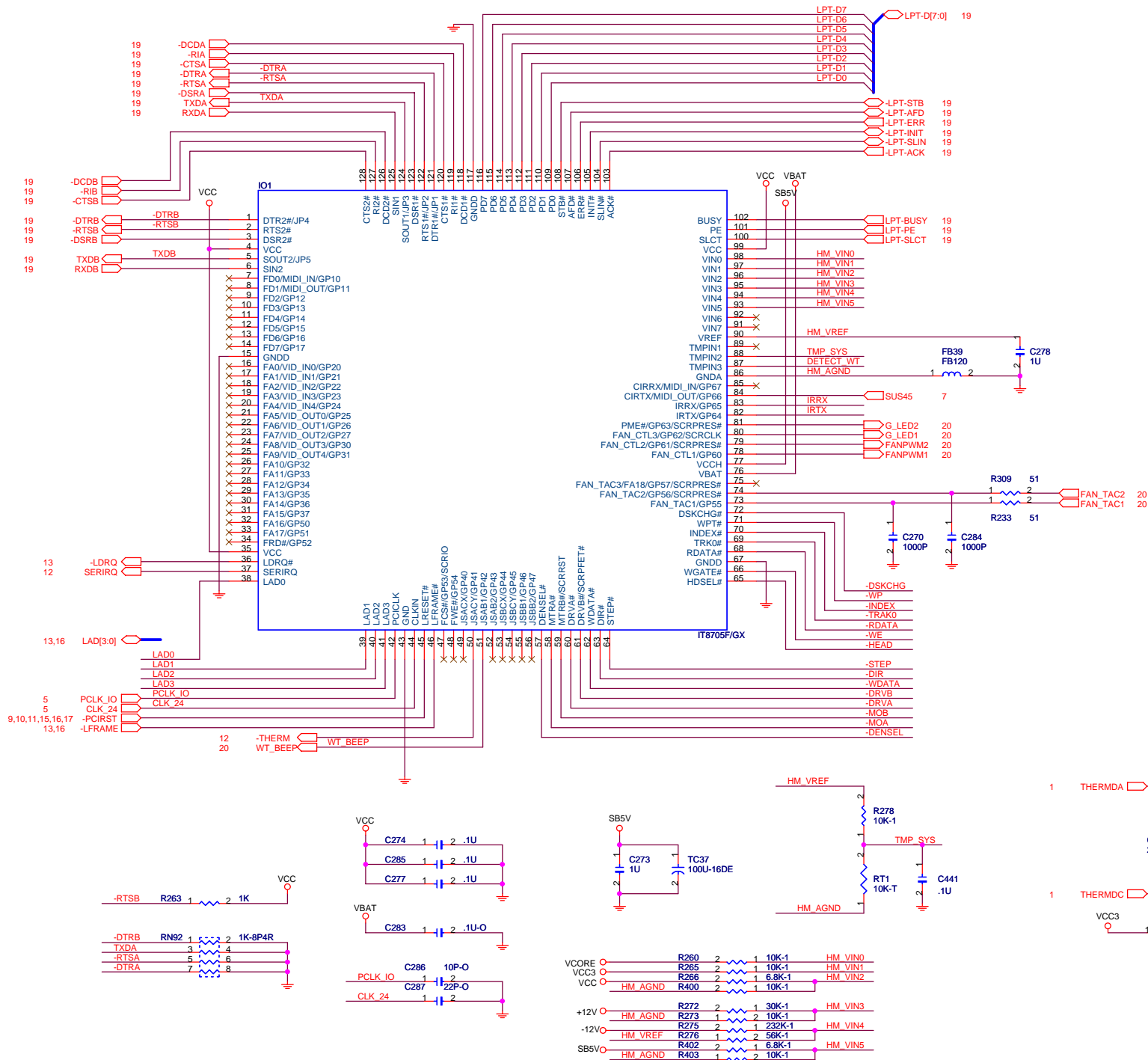




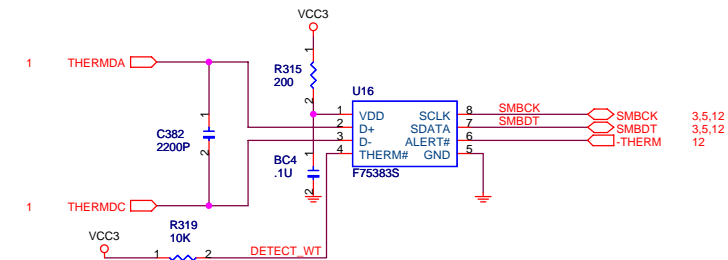
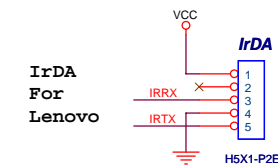
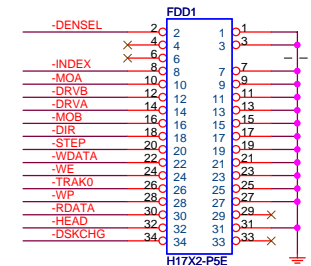
INT:C  
IDSEL:AD21







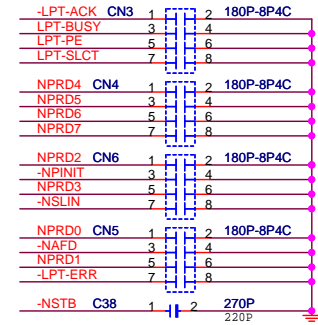
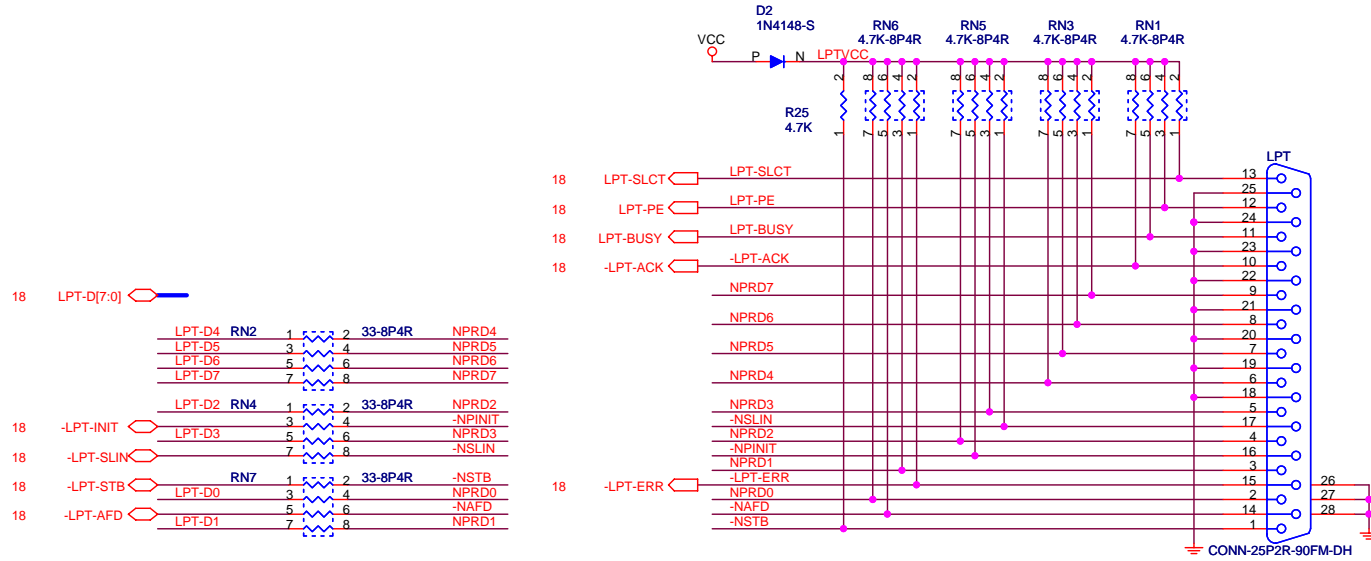
Key pin ( No through hole )



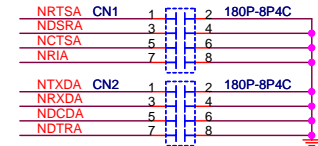
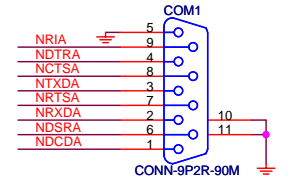
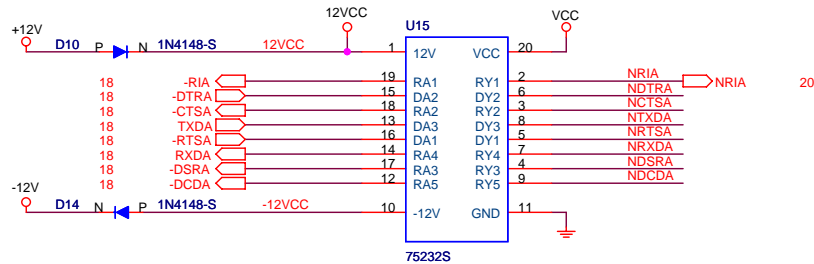
Modify Volt. input for Lenovo request

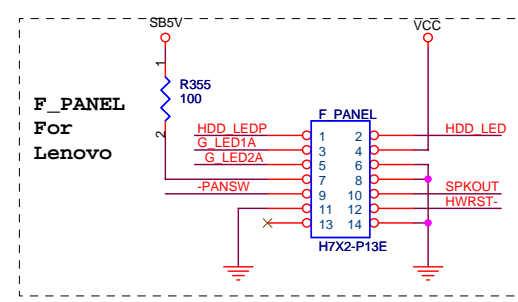
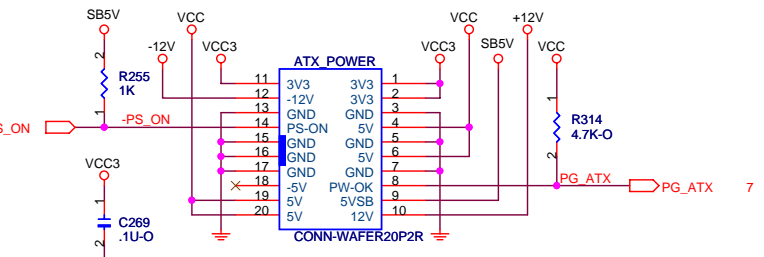
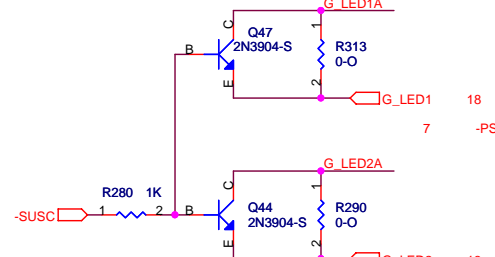
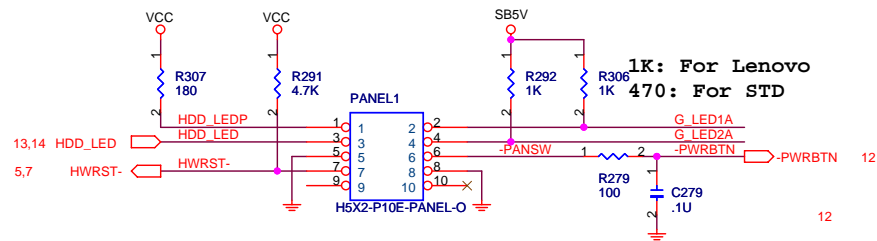
Elitegroup Computer Systems			
LPC SIO - ITE8705			
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# LPT

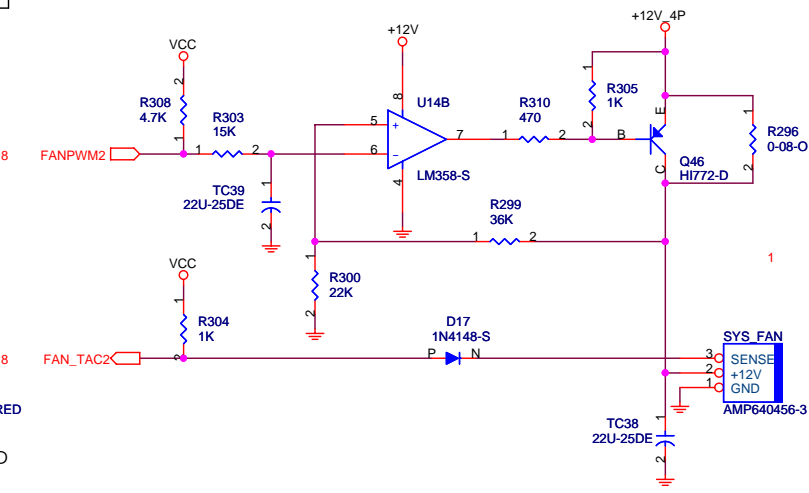
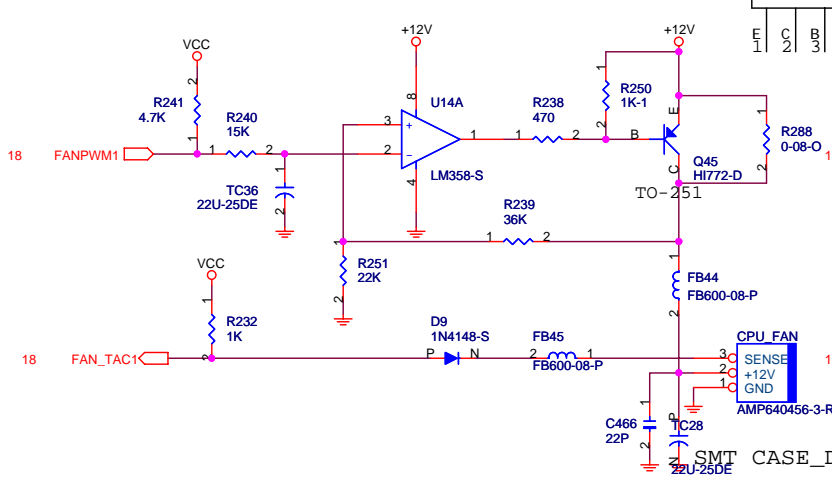
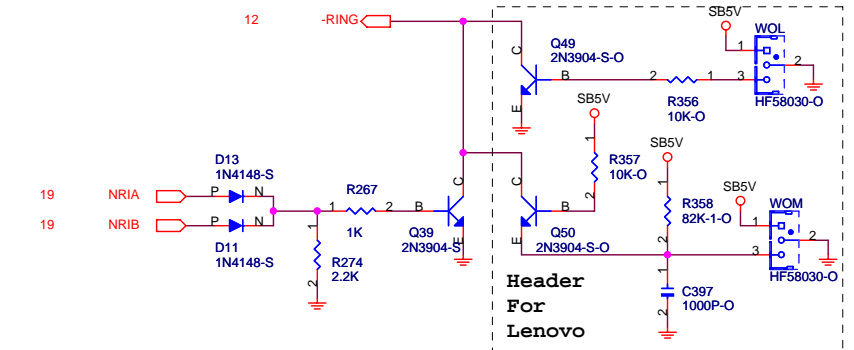
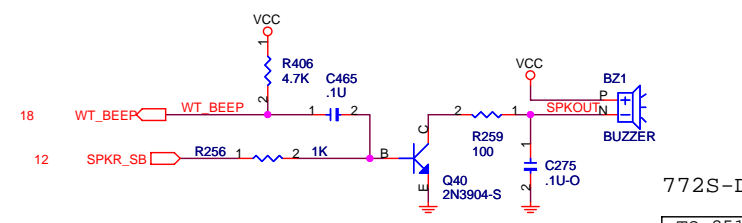
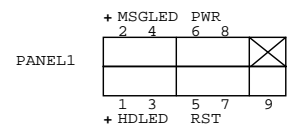
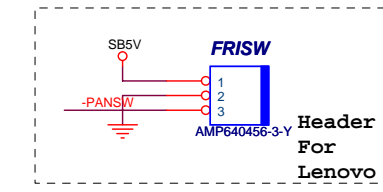
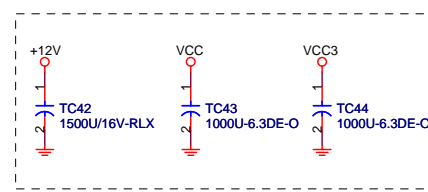


# COM 1\_2





SUSST1#	SUSA#	SUSB#	SUSC#	MODE
0	0	0	0	Mechanical off
1	0	0	0	S4/S5
1	0	0	1	S3
1	0	0	1	S1
1	0	1	1	S0 (ON)

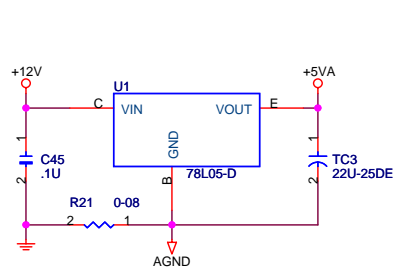


**Elitegroup Computer Systems**

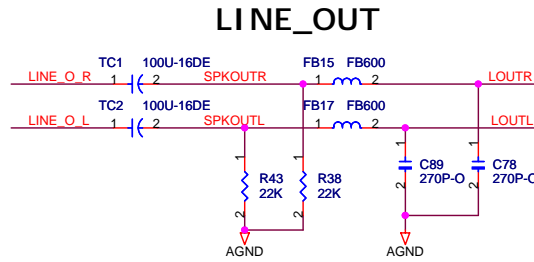
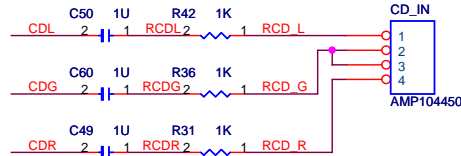
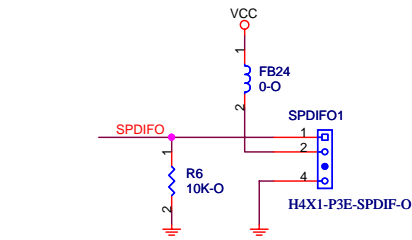
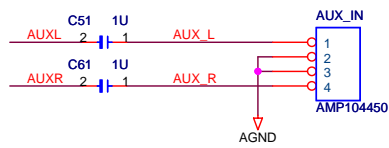
**Front Panel, FAN**

Size: Custom  
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Rev: **1.0A**

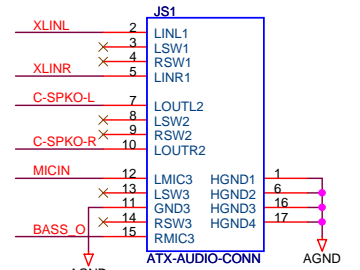
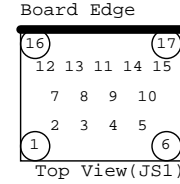
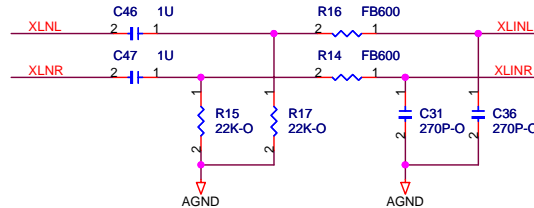




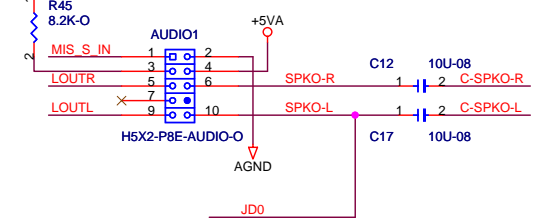
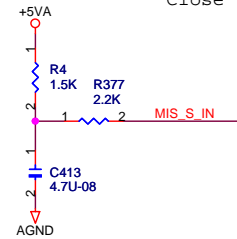
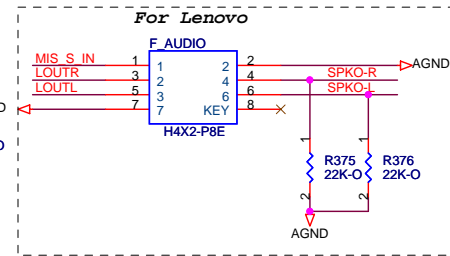
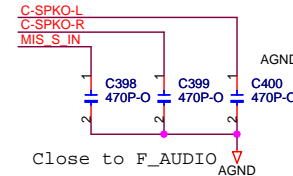
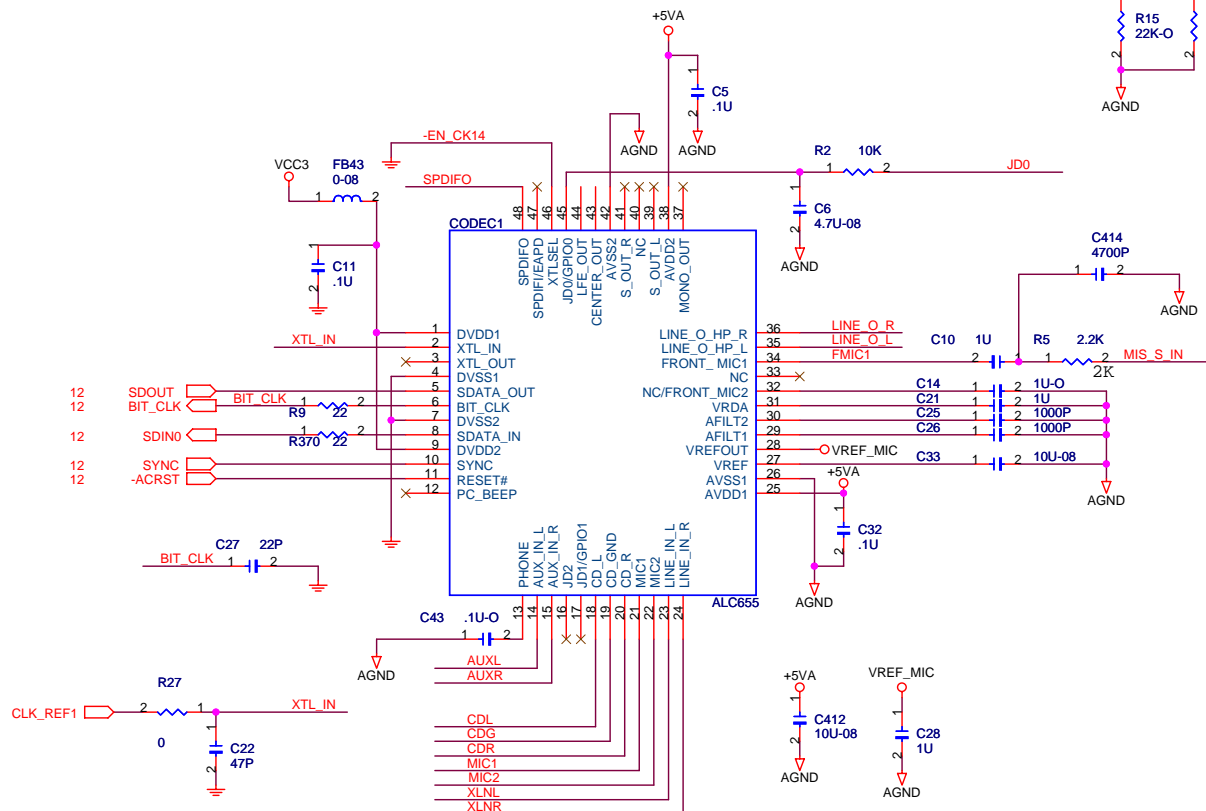
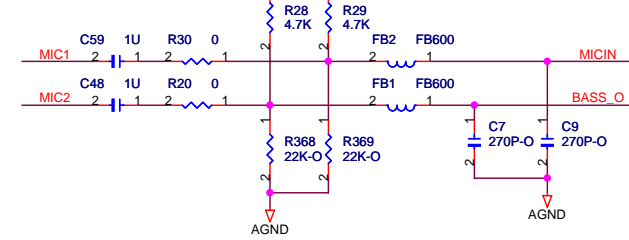
## CD-IN



## LINE\_IN



## MIC\_IN



## Elitegroup Computer Systems

Title			
AC97 CODEC(ALC655)			
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1). Schematics version history table :

Circuit Ver.	PCB Ver.	Total Page	Modificatory Page	Date
A	A	23		10/25/'04
1.0	1.0	23		Jan/10/'05
1.0A	1.0A	23		Nov/18/'05

- 1 K8 - 754 CPU (HT)A,C

2 K8 - 754 CPU (MEM)B,D,E

3 DDR 1,2

4 DDR3, DDR Terminator

5 Clock Generator

6 Power (CPU Vcore)

7 Power (DC to DC)

8 NB - K8M800(HT)A,C

9 NB - K8M800(AGP, VLink, VGA)B

10 AGP SLOT (UAGP3.0) & VGA

11 SB - VT8237A (PCI & USB)

12 SB - VT8237B (IDE & GPIO)

13 SB - VT8237C (VLink, LPC & MII)

14 USB, PS2 & IDE

15 PCI 1, 2
- 16 PCI 3 & LPC ROM

17 LPC SIO - ITE8705

18 COM, LPT

19 Front Panel, FAN

20 AC97 CODEC(ALC655)

21 1394 TI TSB43AB22

22 Cover Page

23 Block Diagram
- Chipset: K8T800(B) rev:CD

Chipset: K8M800 rev:CE

Job	Signature	Date
Schematics Designer	Jeff Hsu	Nov/18/'05
Layout Company	ECS Layout	Nov/18/'05
Approval	Jeff Hsu	Nov/18/'05

# K8M800-M3

Rev: 1.0A

2). Circuit and Layout modification item listing :

- K8M800-M VER: 2.0 ---> K8M800-M3 VER:A
1. RealTek RTL8100C change to VIA PHY 6103L

2. Follow Lenovo K8T800 MB spec.

3. K8T800 Rev:B /K8T800PRO/K8M800 Dual LAY

4. CPU: Dual Sourcing SENSOR

5. Phase in N+P MOS at SO 8P component

3. Modify 1394a chip to Ti-TSB43AB22

7. Phase in to 3in1 USB+LAN+Transformer connector

8. CPU\_FAN/SYS\_FAN change to TO-251 package

9. Add SURGE IC

10. Add Graphics signal level buffer

11. Change PWM vendor to Intersil

- K8M800-M3 VER: 1.0
1. Phase in to 4in1 USB+LAN+Transformer+Surge connector

2. Update the HW monitor circuit

3. Modify PWM circuit by Intesil recommand

4. Avoid TC4 too near with D3/USBLAN1

- K8M800-M3 VER: 1.0.
1. Modify TC28 E/C cap. from DIP to SMD D type for CPU back panel

2. Modify PWM power by Intesil recommand

- K8M800-M3 VER: 1.0A
1. Modify Screw hole power layer

2. Add WEEE logo

Elitegroup Computer Systems

Title

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Document Number

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Cover Sheet

1.0A

Date:

Tuesday, December 20, 2005

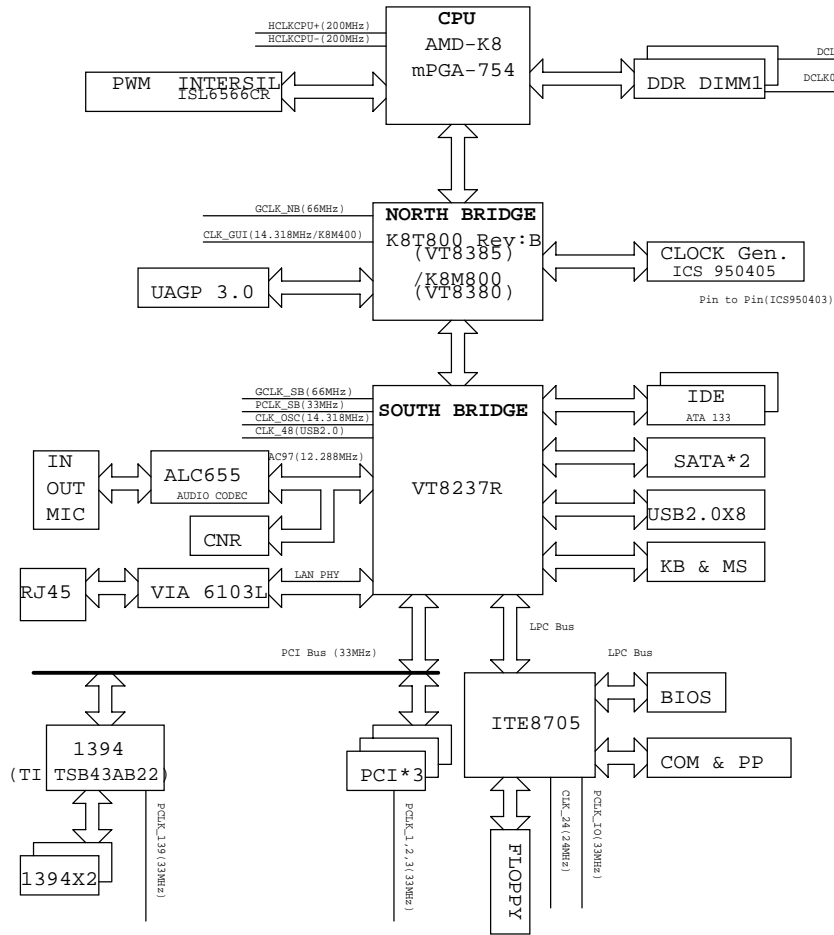
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23

PCB STACK: L1:SIGNAL  
L2:GND  
L3:PWR  
L4:SIGNAL



SB's GPIO

- GPIO14 / 15  
1 1 ---> W / S3  
1 0 ---> W / O S3
- GPO12/13 --- VDDQ Voltage adjust
- GPO20/21 --- VCC25 Voltage adjust
- GPO2 --- FOR IT8282M CONTROL ACPI S3  
Enter S3 to LOW, other status as HIGH
- GPI8 / VGATE --- P66DET
- GPI29 / VRDCLP --- S66DET
- GPO5 / CPUPSTP# --- Control BIOS PROTECT  
LOW ---> PROTECT ENABLE  
HIGH ---> PROTECT DISABLE

8705's GPIO (GX)

- GP41 / PIN50 --- THERM#
- GP62 / PIN80 --- G\_LED1
- GP63 / PIN81 --- G\_LED2

	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking & Yellow	Dark
SV1(1,3)(2,3)	Light	Blinking	Blinking	Dark
LSU1(1,2)	Dark	Dark	Light	Dark
GLE1	HIGH	HIGH	LOW	HIGH
GLE2	LOW	SWITCH	SWITCH	HIGH

- TMPIN2 -> SYSTEM / TMPIN3 -> CPU
- GP66 --- SUS45 for S5 dual power.

CPU(K8): Vcore  
VCC12  
DDRVT  
V\_DIMM  
VCC25A

NB(K8T800): VCC12  
Core voltage V15\_25(K8M800:1.5V)  
VDDQ  
VSUS\_NB  
VCC3(K8M800)

SB(VT8237): VCC25  
VCC3  
VCC25SB  
3VSB

REF. Voltage

	K8M800	K8T800
VL_VREF_NB	0.625V	0.625V
VL_VREF_SB	0.3V	0.625V

	8X	4X
AGPVREF	0.347V	0.75V

MEM_VREF_CPU	1.25V
MEM_VREF_DIM	1.25V

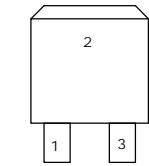
K8 POWER UP SEQUENCE	
K8VTM-A	AMD DESIGN GUIDE
1.-PS_ON	1.-PS_ON
2.DDRVT	2.VTT(DDRVT)
3.V_DIMM	3.VDDIO(V_DIMM)
4.VCC25A	4.VDDA(VCC25A)
5.VCORE	5.VDD(VCORE)
6.VCC12	6.VLDT(VCC12)
	7.PWROK

	(Default)	Impedance	PCB 2116
USB_DT0+/-	(45/90)		8/8/8(47/87)
LAN RX+/- TX+/-	(50/100)		8/10/8(47/89)
S-ATA	(50/100)		6/6/6(56/98)
1394	(55/110)		6/9/6(56/105)
R.G.B	(37.5)		50/9/9/9/9/50 Put 75 ohm on CON

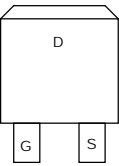
PCI Bus Resource				
PCI1	AD19	INTA,BCD	REQ0	GEN-PIN13
PCI2	AD20	INTB,CDA	REQ1	GEN-PIN14
PCI3	AD21	INTC,DAB	REQ2	GEN-PIN17
Ti	AD25	INTC	REQ4	GEN-PIN24

# LPC ROM ---> GEN-PIN18

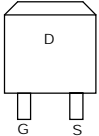
22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
220U/16DE	6*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



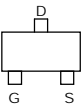
TO-263  
55N03L(55A,14m,25V)



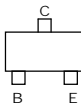
TO-263  
15N03(42A,12.6m,30V)  
2SK3296(35A,12m,20V)



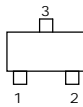
TO-252  
55N03(55A,14m,25V)  
20N03(30A,20m,30V)  
45N03(45A,30m,30V)  
TM3055TL-S(8A,90m,30V)  
FDD6030L(50A,14,5m,30V)



SOT-23  
2N7002  
SI2303S  
SI2301S



SOT-23  
2N3904  
2N3906  
MMBT2907A



SOT-23  
BAT54C  
BAT54S



TO-92  
LM431  
78L05-D  
LM432



TO-92  
2N2222A  
2N2097A(0.6A)  
HA8550(1.5A)

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Block Diagram				Rev
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